

# Ramniranjan Jhunjhunwala College of Arts, Commerce and Science (Empowered Autonomous) Ghatkopar (W), Mumbai 400086

**SYLLABUS FOR SEM - V Program: B.Sc. Physics Major - DSE** 

**Course Code:** 

Sem V: RJDSEPHY351, RJDSEPHY352, RJDSEPHY9352

Sem VI : RJDSEPHY361, RJDSEPHY362, RJDSEPHYP362

# Credit Based Semester System w. e. f. the Academic Year 2025 –2026

Syllabus for T.Y.B.Sc. Physics Major (Choice Based Credit System w. e. f. academic year 2025-26 in compliance with NEP 2020)

The revised syllabus in Physics as per credit based system for the Sem 3 B.Sc. Course will be implemented from the academic year 2025–2026. The syllabus is for the Semester V, Physics Major course. The systematic and planned curricula from these courses shall motivate and encourage learners to understand basic concepts of Physics. The National Education Policy 2020 aims at imparting skill-based learning and caters to the multiple entry and exit facility for the students thus empowering them to acquire knowledge at their pace In the three-year UG program, the student has two exit options. Students also have the option of choosing the Honors program of four years of study in each discipline and later converting it to a five-year integrated PG degree program. As an undergraduate student, he/she learns the core subject (Major), a subject complementing the core subject (Minor), a course from another discipline (OEC or GEC), Vocational and Skill Enhancement course from the Major (VSEC). The remaining verticals under NEP 2020 are IKS (Indian Knowledge System), AEC (Ability Enhancement Course), VEC (Value Education Course) and with progressive three years of UG. A student also completes at different levels OJT (On Job Training), FP (Field Projects), CEP (Community Engagement Project), RP (Research Project) which helps him/her in understanding their roots, application of the knowledge for the benefit of self and the society. Vertical CC (Co-curricular activities and activities related to yoga and human well-being) helps in preparing youth with good character and interpersonal relationships.

#### **Objectives:**

- To develop analytical abilities towards real world problems.
- To familiarize with recent scientific and technological developments.
- To enrich knowledge through problem solving, hands-on activities, study visits, projects etc.

Course code	Title	Credits	Remarks
	Semester V		
RJDSEPHY351	Analog Electronics	2	
RJDSEPHYP351	Analog Electronics Laboratory	2	
RJDSEPHY352	Computational Physics I	2	
RJDSEPHYP352	Computational Physics Laboratory 1	2	

Course code	Title	Credits	Remarks
	Semester VI		
RJDSEPHY361	Digital Electronics	2	

Course code	Title	Credits	Remarks
	Semester VI		
RJDSEPHYP361	Digital Electronics Laboratory	2	
RJDSEPHY362	Computational Physics-II	2	
RJDSEPHYP362	Computational Physics Laboratory 2	2	

## **SEMESTER-V**

Name of the Program	Duration	Semester	Subject
B.Sc. in Physics/Honors	6/8 semesters	V	Physics
Course Code	Title		
RJDSEPHY351	<b>Analog Electronics</b>		
RJDSEPHYP351	Analog Electronics		
	Laboratory 1		

## **Evaluation scheme:**

Internal Assessment (continuous evaluation)	Semester End Exam	
40%	60%	
Will consist of tests, assignments, projects, participation and other schemes with the permission and suggestions of the Exam Committee.	Written exam with a marking scheme suitable to the topics. This marking scheme / paper pattern will be discussed by the teacher while conducting the course.	
The evaluation scheme may be modified as per suggestions and instructions of the Exam Committee.		

#### **Course Outcomes:**

On successful completion of this course students will be able to:

- 1. Understand the Transistor Multivibrators
- 2. Understand the working of JFET and MOSFET
- 3. Use Op-Amp in applications
- 4. Understand the working of 555 Timer
- 5. Use IC 555 in applications

	SEMESTER V				
Disc	Discipline Specific Elective Physics RJDSEPHY351 Analog Electronics				
Unit I		15 hours			
1.	Transistor Multivibrators:  Transistor as a switch: Transistor Characteristics, operating				
	point, cut-off region, saturation region, Transistor as a switch and as an inverter MB: 6.6, 7.2, 7.3, 7.5 AM: 18.9 Transistor Multivibrators: Astable, Monostable and Bistable Multivibrators, Schmitt trigger. (ZM: Basic Electronics – A text Manual Zbar and Malvino-TMH or AM) AM: 18.11				
2.	Field effect transistors:  JFET: Basic ideas, Drain curve, The transconductance curve, Biasing in the ohmic region and the active region, Transconductance, JFET common source amplifier, JFET analog switch – multiplexer and chopper, voltage controlled resistor MB: Art. 13.1 to 13.9  MOSFET: Depletion and enhancement mode, MOSFET operation and characteristics, sample and hold amplifier, CMOS Inverter MB: Art. 14.1, 14.2, 14.4, , 14.7, VKM: Art. 19.28, 19.29, 19.30, 19.31, 19.32, 19.36				
Unit II		15 hours			

1.	Op-amp: Introduction, ideal Characteristics of Op-amp, Virtual Ground Concept Applications of Op-Amps: Inverting amplifier, Non inverting amplifier, Voltage Follower, summing amplifier, Applications of Summing Amplifier, Differential Amplifier, integrator, Critical frequency of integrators, differentiator, Log amplifier, Comparators, Comparator Circuits: Schmitt Trigger, Astable using Op-amp, square wave and triangular wave generator using Op-amp, Wein-bridge oscillator using Op-amp, First order Active low pass filter and high pass filter, Second order Active Band pass filter and Band stop filter.  VKM: Articles: 25.1, 25.15, 25.16, 25.19, 25.20, 25.23, 25.24, 25.26, 25.27, 25.32, 25.33, (MB: Art. 20.4), 25.34, 25.35, 25.36, MH: 16.14, 25.37, 25.38, 25.39		
2.	555 Timer: Basic timing diagram, 555 Block diagram, Monostable and Astable operation (with VCO), Schmitt Trigger, Bistable, Triggered linear ramp generator.  MLS: Art. 7.3 to 7.5.  MB: Art. 23.7 to 23.9		
References:	<ol> <li>MB: Electronic Principles: A. P. Malvino and D.J. Bates (7th Ed.) – (TMH).</li> <li>VKM: Principles of Electronics: V. K. Mehta and Rohit Mehta.</li> <li>Chand Publications. (11th Ed.).</li> <li>MLS: Digital Principles and Applications: Donald Leach, A Malvino, Goutam Saha (13th Edition) (McGraw Hill Publication)</li> <li>MH: Integrated Electronics: Millman and Halkias McGraw Hill International.</li> </ol>		
Additional References:	1. Electronic Devices and Circuits: S. Salivahanan, N. Suresh Kumar and A. Vallavaraj. (2nd Ed.) (Tata McGraw Hill) 2. Pulse, Digital & Switching Waveforms: Millman & Taub (TMH) 3. AM: Electronic devices and circuits – An introduction Allan Mottershead (PHI Pvt. Ltd. – EEE – Reprint – 2013) 4. BN: Electronic Devices And Circuit Theory: Robert Boylestad and Louis Nashelsky (7th/8th Edition Prentice Hall) 5. KVR: Functional Electronics: K.V. Ramanan (TMH).		
Discipline Specific Elective Physics RJDSEPHYP351 Analog Electronics Laboratory			
Practicals :	<ol> <li>Transistorized Astable multivibrator</li> <li>Transistorized Bistable multivibrator</li> <li>Transistorized Monostable multivibrator.</li> <li>FET characteristics</li> <li>Op-amp – Inverting amplifier with different gains</li> <li>Op-amp – Non-inverting amplifier with different gains</li> <li>Op-amp – Difference Amplifier</li> </ol>		

	8. Op-amp – Summing Amplifier 9. Op-amp – Differentiator 10. Op-amp – Integrator 11. Schmitt trigger using Op-amp. 12. Log amplifier using Op-amp 13. First order Low pass filter Using Op-amp 14. First order high pass filter Using Op-amp 15. Second order Band pass filter using Op-amp 16. Second order Band stop filter using Op-amp 17. Wien Bridge Oscillator Using Op-Amp 18. 555 Timer Astable multivibrator 19. 555 Timer as Monostable multivibrator 20. 555 Timer as Schmitt Trigger. 21. 555 Timer as ramp generator.	
Skill:	<ol> <li>Transistor as a switch and an Inverter</li> <li>Voltage follower using Op-amp</li> <li>Inverter using Op-amp</li> <li>Op-amp as comparator</li> <li>555 Timer as a bistable multivibrator.</li> </ol>	
Demonstratio n:	<ol> <li>Waveform generator using Op-amp (Sine Wave, Square Wave and Triangular)</li> <li>Instrumentation Amplifier using Op-Amp</li> <li>Analog Multiplier using Op-amp</li> </ol>	

# **SEMESTER-V**

Name of the Program	Duration	Semester	Subject
B.Sc. in Physics/Honors	6/8 semesters	V	Physics
<b>Course Code</b>	Title		
RJDSEPHY352	Computational		
	Physics I		
RJDSEPHYP352	Computational		
	Physics Laboratory I		

## **Evaluation scheme:**

Internal Assessment (continuous evaluation)	Semester End Exam
70%	30%
Will consist of tests, assignments, projects, participation and other schemes with the permission and suggestions of the Exam Committee.	Written exam with a marking scheme suitable to the topics. This marking scheme / paper pattern will be discussed by the teacher while conducting the course.

The evaluation scheme may be modified as per suggestions and instructions of the Exam Committee.

	SEMESTER V			
Discipl	Discipline Specific Elective Physics RJDSEPHY352 Computational Physics I			
Unit I	Monte Carlo Simulation	15 hours		
1.	Integrating equation of motion of a few variables, three-body problem, role of molecular dynamics (MD), the basic machinery, Lennard-Jones potentials modeling physical system, boundary conditions, time integration algorithm, starting a simulation, simulation of microcanonical (NVE) and canonical ensemble (NVT), controlling the system (temperature, pressure), thermostats and barostats, equilibration, running, measuring and analyzing MD simulation data, measurement of statistical quantities, interatomic potentials, force fields.			
Unit II	Molecular Dynamics Simulation	15 hours		
1.	Random number: Definition, True and Pseudo random number generators (RNG), uniform and non-uniform RNG, Linux RNG, testing a RNG. Monte Carlo simulation: Buffon's needles, MC Integration, hit and miss, stochastic processes, sample mean integration, important sampling, Markov Chain, Metropolis method, master equation, introduction to 2d-Ising model. Random walk: two dimensional random walk, calculation of rms displacement.			
Discipline Specific Elective Physics RJDSEPHYP352 Computational Physics I Laboratory				
	Related Programs on Monte Carlo Simulation	60 hours		

	1. Pi Estimation	
	2. Coin Toss Simulation	
	3. Random Walk Simulation	
	4. Minimization of a Function	
	5. Maximization of a Function	
	6. Traveling Salesman Problem	
	7. Monte Carlo Tree Search	
	8. Poker Simulation	
	Related Programs on Molecular Dynamics Simulation	
	1. Simple Harmonic Oscillator	
	2. Lennard-Jones Potential	
	3. Molecular Collision Simulation	
	4. Ideal Gas Simulation	
	5. Temperature and Pressure Simulation	
	6. Phase Transition Simulation	
	7. Molecular Visualization using Matplotlib or VTK.	
	8. Trajectory Analysis: mean squared displacement.	
References:	1. A Molecular Dynamics Primer, Furio Ercolessi,	
	http://www.fisica.uniud.it/~ercolessi/md/	
	2. Understanding Molecular Simulation, Daan Frenkel and B.	
	Smit, Academic Press, 1996.	
	3. Computational Physics, J. M. Thijssen, Cambridge Univ.	
	Press, 1999.	
	4. Molecular Dynamics Simulation- Haile (Wiley	
	Professional)	
Additional	1. A first course in computational Physics, Paul, L. Pavries,	
References:	Pub. John Wiley and Sons, 1994.	
	2. Monte Carlo Methods, M. H. Kalos and P. A. Whitelock,	
	John Wiley & Sons, NY 1986.	
	3. A Guide to Monte Carlo Simulations in Statistical Physics	
	- Landau & Binder (Cambridge University Press).	
	4. Statistical Mechanics - Algorithms and Computations -	
	Krauth (Oxford University Press).	
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Duration	Semester	Subject	Credits
6/8 semesters	VI	Physics	4
		-	
Title			
<b>Digital Electronics</b>			
Digital Electronics			
	6/8 semesters  Title  Digital Electronics	6/8 semesters VI  Title Digital Electronics Digital Electronics	6/8 semesters VI Physics  Title Digital Electronics  Digital Electronics

#### **Course Outcomes:**

On successful completion of this course students will be able to:

- 1. Understand the Binary number system, logic gates, Boolean Algebra, logic circuits
- 2. Use methods of designing logic circuits
- 3. Construct digital systems
- 5. Understand the working of flip-flops, counters and registers

# **Learning Outcomes:**

#### **Evaluation scheme:**

Internal Assessment (continuous evaluation)	Semester End Exam	
40%	60%	
Will consist of tests, assignments, projects, participation and other schemes with the permission and suggestions of the Exam Committee.	Written exam with a marking scheme suitable to the topics. This marking scheme / paper pattern will be discussed by the teacher while conducting the course.	
The evaluation scheme may be modified as per suggestions and instructions of the Exam Committee.		

SEMESTER VI		
Physics Discipline Specific Elective RJDSEPHY361 Digital Electronics		
Unit I Combinational Logic Circuits 15 hours		

	Number Systems: Binary number system, Binary to decimal and decimal to binary conversion, Number representation in binary: Unsigned, Sign Magnitude, 1's Complement, 2's Complement  Digital Arithmetic: Binary addition, Binary Subtraction, Addition using the 2's Complement Method, Subtraction using the 2's Complement Arithmetic  Logic Gates: OR, AND, NOT, NAND, NOR, EX-OR gates, NAND and NOR as basic building blocks in logic circuits Boolean Algebra: Boolean laws, De Morgans and Duality theorems, SOP method, POS method, Karnaugh Map,  Arithmetic Circuits: Half adder and Full adder, Half subtractor and Full subtractor, Controlled Inverter, Adder-Subtractor, One bit comparator, and 2-bit comparator, Multiplexer and De-multiplexer, Decoder and Encoder.	
	AKM: 1.4, 1.9.1, 1.10, 1.8, 1.8.1, 1.8.2, 1.8.3, 3.1, 3.2, 3.2.1, 3.3, 3.3.1, 4.3, 4.3.1, 4.3.2, 4.3.3, 4.3.4, 4.3.5, 4.3.6, 4.4, 4.5, 6.1, 6.1.1, 6.1.2, 6.1.3, 6.2, 6.3, 6.3.1 to 6.3.14, 6.3.17, 6.4.1, 6.4.2, 6.6, 6.6.1, 7.3.1, 7.3.2, 7.3.3, 7.3.4, 7.3.5, 7.4, 7.9, 8.1, 8.3, 8.2  LMS: 5.1, 5.3, 5.5, 6.3, 6.4, 6.5, 6.1, 6.2, 6.6, 2.1, 2.2, 3.1,	
	3.2, 3.7, 3.3 to 3.6, 6.7, 6.8, 4.9, 4.1, 4.2, 4.3, 4.6	
Unit II	Sequential Logic Circuits	15 hours
	<b>Flip-flops:</b> Basic R-S flip-flop, Clocked R-S flip-flop, Level triggered and Edge triggered flip-flop, J-K Flip-flop, Master-Slave J-K Flip-flop, T Flip-flop, D Flip-flop, Contact debounce circuit,	
	Counters: Binary Ripple Counter, Up mode, Down mode, Up/Down counter, Modulus N Counters (N<2 <sup>n</sup> ), Modulo (N1xN2) counter, Mod 3x2 counter, Mod 2x3 counter, Mod 5x2 counter, Mod 2x5 counter, BCD decade counter, Cascaded BCD decade counter, Synchronous Counter	
	Registers: Shift Register, Serial-In Serial-Out Shift Register, Serial-In Parallel-Out Shift Register, Parallel-In Serial-Out Shift Register, Parallel-In Parallel-Out Shift Register	

	AKM: 10.3, 10.3.1, 10.3.2, 10.3.3, 10.4, 10.5, 10.5.1, 10.5.2, 10.6, 10.6.1, 10.7, 10.7.1, 10.7.2, 10.10.1, 11.1, 11.4, 11.6, 11.3, 11.4.1, , 11.7, 11.10.2, 11.2, 11.5, 11.12, 11.12.1, 11.12.2, 11.12.3, 11.12.4, LMS: 8.1, 8.2, 8.5, 8.8, 8.9, 10.1, 10.3, 9.1, 9.2, 9.3, 9.4, 9.5	
References:	AKM; Digital Electronics Principles, Devices and Applications, Anil K. Maini, John Wiley & Sons, Ltd     LMS: Digital principles and applications (8 <sup>th</sup> Edition) Leach, Malvino and Saha–TMH	
Additional References:	<ol> <li>Fundamental of Digital Electronics Digital Techniques C.         V. Dhuley and V. M. Ghodki, Lambert Academic Publishing</li> <li>Digital Electronics and logic design, B. S. Nair, Prentice Hall India</li> <li>Digital Computer Electronics 3<sup>rd</sup> Edition Malvino, Brown Tata McGraw Hill</li> </ol>	
Physics Disc	cipline Specific Elective RJDSEPHYP361 Digital Electronics	Laboratory
Practicals:	1) Study of Logic Gates (OR, AND, NOT, NAND, NOR, EX-OR). 2) Study of NAND and NOR as universal gates. 3) Verification of De Morgan's Theorems. 4) Verification of Boolean laws and duality Theorem. 5) Study of Ex-OR gate using basic logic gates. 6) Study of half adder and full adder 7) Study of half subtractor and full subtractor 8) Study of 1-bit comparator and 2-bit comparator IC 7485 9) Study of Multiplexer IC 74151 10) Study of De-multiplexer IC 74138 (/ IC 74237) 11) Study of Decoder IC 74138 12) Study of Encoder IC 74148 13) Design and study an S-R flip-flop using NOR/ NAND gates 14) Study of M/S J-K flip-flop IC 7473 15) Study of D type flip-flop and T type flip-flop using JK flip-flop 16) 3 bit Ripple up and down counter using JK flip-flop IC 7476 17) Modulo N counter using IC 7476 or IC 7490 ( N=10) 18) 3 bit (mod-8) Synchronous up and down counter using JK flip-flops IC 7476 19) Study of Shift register IC 7495	

Skill:	<ol> <li>4-bit controlled inverter</li> <li>Study of D flip-flop using RS flip-flop or IC 7474</li> <li>n number of T- type flip-flops as divided by 2<sup>n</sup> circuit for input frequency.</li> </ol>	
Demonstrati on :	<ol> <li>BCD Adder</li> <li>Decade counter IC 7490</li> <li>4-bit binary counter IC 7493</li> </ol>	

Name of the	Duration	Semester	Subject	Credits
Program				
B.Sc. in	6/8 semesters	VI	Physics	2
Physics/Honors				
Course Code	Title			
RJDSEPHY362	Computational			
	Physics-II			
RJDSEPHYP362	Computational			2
	Physics-II Laboratory			

## **Evaluation scheme:**

Internal Assessment (continuous evaluation)	Semester End Exam
70%	30%
participation and other schemes with the permission and suggestions of the Exam	Written exam with a marking scheme suitable to the topics. This marking scheme / paper pattern will be discussed by the teacher while conducting the course.

The evaluation scheme may be modified as per suggestions and instructions of the Exam Committee.

Physics Paper 4 RJDSEPHY362 Computational Physics -II		
Unit I	Fine difference and element methods for PDEs	15 hours
1.	Introduction of PDE, Classification of PDE: parabolic, elliptic and hyperbolic. Boundary and initial conditions, Taylor series expansion, analysis of truncation error, Finite difference method: FD, BD & CD, Higher order approximation, Order of Approximation, Polynomial fitting, One-sided approximation, solution to each type of PDE by one chosen methods.	
Unit II	Optimisation Techniques	15 hours
1.	Definition and importance of optimization, Types of optimization problems (linear, nonlinear, discrete, continuous), applications of optimization techniques  Gradient Descent: Introduction, convergence, and variants (e.g., stochastic gradient descent), Newton's Method: Introduction, convergence, and limitations, Quasi-Newton Methods (e.g., BFGS): Introduction and convergence, Conjugate Gradient Method: Introduction and convergence  Introduction to LP and its formulation, Simplex Method: Step-by-step process and examples, Interior Point Methods: Introduction and convergence  Introduction to NLP and its formulation, Unconstrained Optimization: Using gradient descent and Newton's method, Constrained Optimization: Using Lagrange multipliers and penalty methods	

References:	<ol> <li>Computational Physics, J. M. Thijssen, Cambridge Univ. Press, 1999.</li> <li>"Numerical Analysis" by Richard L. Burden and J. Douglas Faires</li> <li>"Computational Methods for PDEs" by S. McKee and M. A. Johnson</li> <li>"Optimization: Algorithms and Applications" by Meir J. Rosenblatt</li> <li>"Introduction to Optimization" by Jim Burke</li> <li>"Computational Optimization: An Introduction to Numerical Methods" by Michael S. Bartholomew-Biggs</li> </ol>	
Disciplin	ne Specific Elective Physics RJDSEPHYP362 Computational Laboratory	Physics II
Programs	Finite Difference Methods	60 hours
	1. Heat Equation in 1D	
	2. Wave Equation in 1D	
	3. Laplace Equation in 2D	
	Finite Element Methods	
	1. Poisson Equation in 2D	
	2. Heat Equation in 1D	
	3. Wave Equation in 1D	
	Optimization	
	Optimization - Gradient descent	
	1 -	
	- Gradient descent	
	- Gradient descent - Newton's method	
	<ul><li>Gradient descent</li><li>Newton's method</li><li>Quasi-Newton methods (e.g., BFGS)</li></ul>	

## Ramniranjan Jhunjhunwala College (Empowered Autonomous), Ghatkopar West RULES AND REGULATIONS REGARDING ASSESSMENT AND EVALUATION FOR FY UNDER NEP FROM A.Y. 2023-2024 ONWARDS-

- 1. A learner appearing for first year examination under NEP will have **maximum of 22 credits** and examinations will be of **maximum 550 marks**.
- 2. Courses having 2 credits, 3 credits and 4 credits will have examinations of 50, 75, 100 marks respectively.
- 3. With regard to Major Course, Minor Course and OEC:

**Continuous evaluation** of 40-60 adopted under autonomy (2018) shall continue for all the courses; for the courses with 2 credits and 50 marks, Internal is of 20 marks (only one IA) and External 30 marks (SEE); while the courses with 3 credits and 75 marks, it is 25 marks (only one IA) and 50 marks (SEE). In case of courses of 100 marks, the break up of marks will be 40 marks (IA) and 60 marks (SEE).

## 4. With regard to IKS, VSEC (VSC and SEC), AEC, VEC:

These will be of 2 Credits each and of 50 marks. Continuous evaluation of 40-60 wherein Internal is of 20 marks and SEE of 30 marks or Only one SEE of 50 marks or continuous evaluation of more than one test by the respective coordinating department or as directed by the EC.

## 5. With regard to CC:

Vertical of CC shall also be more like a **continuous evaluation** where a student will be awarded marks on the basis of **his / her participation in the co-curricular activities of the department / other departments / associations / extension activities / intercollegiate events and Jeevan <b>Kaushal**. A workbook will be provided to a student to keep a record of his / her participation and will be duly signed by the concerned teachers.

### 6. Duration of examinations:

- a. An IA exam of 20/25 marks shall be of duration of 30 minutes.
- b. An SEE exam of 30 marks (offline) shall be of duration of 1 hour.
- c. An SEE exam of 50 marks (offline) shall be of duration of 1 ½ hour.
- d. An SEE exam of 50 marks (online MCQ) shall be of 60 minutes.
- e. An SEE exam of 60 marks (offline) shall be of duration of 2 hours.
- 7. There shall be combined passing of Internals and SEE in a given paper with a minimum passing percentage of 40.
- **8**. **Appearing for SEE** for every paper is **compulsory** irrespective of the performance in the Internals examinations. A student absent in SEE will be thus declared failing in a given subject.
- **9**. There shall be provision for supplementary examination for the benefit of students who miss their SEE on grounds of medical emergency or representing college at the national level event or any other equivalent event with a special permission granted by the Head of the institution.

- 10. There shall be no Additional Examinations for any of the Semesters except for the Semester V wherein one chance of credit improvement in Semester V shall be given before the Learner appears for the final Semester VI Examination.
- 11. A learner appearing for first year exam under NEP shall have examination of maximum 550 marks to which effect ATKT is allowed for maximum of 200 marks corresponding to failing in 3 / 4 courses but must have passed in at least one Theory course of Major / Minor.

#### FOR SY AND TY-

- 12. For the SY (2023-2024) and TY (2023-2024 and 2024-2025) programs, 40 60 pattern of continuous evaluation continues. However, Internal 40% as 20 + 20 is revised from AY 2023-24 as 15 + 25 wherein, 15 marks of assignment and 25 marks of MCQs or any other mode of evaluation as decided by the respective department shall be implemented. Rest of the Rules and Regulations continues as earlier.
- 13. Ordinances 5042A, 5043A & 5044A, 5045A, 5046A, 5048A&B, 5049A, 5050A and 0.229A adopted under autonomy are to accepted as its under NEP. (Next Page)

#### ORDINANCES ADOPTED ON EXAMINATIONS CONDUCTED UNDER AUTONOMY

ORDINANCE NUMBER	MATTER OF REFERENCE	
5042A	Grace Marks for passing in each head of passing	
	(Theory/ Practical/ Oral/ Sessional)	
5043A, 5044A	Grace marks for getting higher Class/ Grade (Grade Jump)	
5045A	Condonation	
5046A	Moderation	
5048A&B	Amendments of Results (Due to errors, Due to fraud, malpractices	
	etc.)	
5049A	Appointment of paper setters, Examiners, Senior supervisors	
	and conduct of examination etc.	
5050A	Ordinance regarding Unfair means resorted to by the Student	
0.229A	Benefit of 10 marks under NSS/ NCC/ LLLS/ SPORTS	

#### Explanation:

**Ordinance 5042A**: the benefit of gracing of marks under the ordinance shall be applicable only if the candidate passes the entire examination of semester/year.

**Ordinance 5043A, 44A**: the benefit of gracing of marks under the ordinance shall be applicable only if the candidate passes in all the subjects and heads of the examination without the benefit of either gracing or condonation rules and shall be given for maximum of 1% of the aggregate marks of the examination or up to 10 marks, whichever is less.

**Ordinance 5045A**: the benefit of gracing of marks under the ordinance shall be applicable only if the candidate fails in only one head of passing and his/her deficiency of marks in such head of passing may be condoned by not more than 1% of the aggregate marks of the examination or 10% of the total number of marks of that head of passing in which he/she is failing, whichever is less.

Condonation of deficiency of marks be shown in the statement of marks in the form of asterisk and Ordinance number.

**Ordinance 5046A**: the ordinance shall be applicable as per the detailed scheme of moderation released by the University of Mumbai via its adaptation in totality.

Where marks awarded by the moderator vary from those awarded by original examiner, the marks awarded by the moderators shall be taken as final.

**Ordinance 5048A&B**: section (A) of the ordinance is applicable to the case where it is found that the result of an examination has been affected by errors, the Controller of Examination shall have power to amend such result provided the errors are reported/detected within 6 months from the date of declaration.

Error means –

- (a) Error in computer/data entry, printing or programming and the like.
- (b) Clerical error, manual or machine in totalling or entering of marks on mark list/register.
- (c) Error due to negligence or oversight of examiner or any other person connected with evaluation, moderation and result preparation.

Section (B) of the ordinance is applicable in any case where the result of an examination has been ascertained and published and it is found that such result has been affected by any malpractices, fraud or any other improper conduct whereby an examinee has benefited and that such examinee has been party of privy to or connived at such malpractice, fraud or improper conduct.

**Ordinance 5049A**: the ordinance shall be applicable as per the guidelines of University of Mumbai. **Ordinance 5050A**: the convener of the Unfair means committee shall take appropriate disciplinary action against the student/s using, attempting to use, instigating or allowing to use unfair means at the examination applying the ordinance as per the guidelines of University of Mumbai.

**Ordinance 0.229A**: the ordinance shall be applicable to the candidate for his/her satisfactory completion of NSS/NCC/DLLE/SPORTS. Benefit of 10 marks be shown in the Statement of Marks in the form of hashtag and Ordinance number.

Dr. Himanshu G. Dawda Principal, Chief Controller of Examination Maj. Pravin G. Nayak Controller of Examination